

FIGURE 1

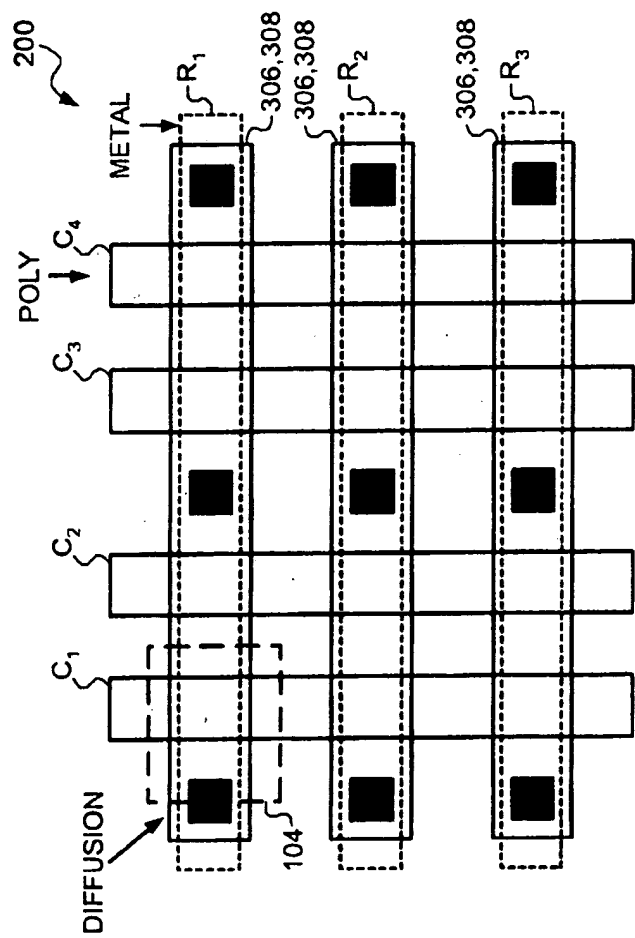


FIGURE 2

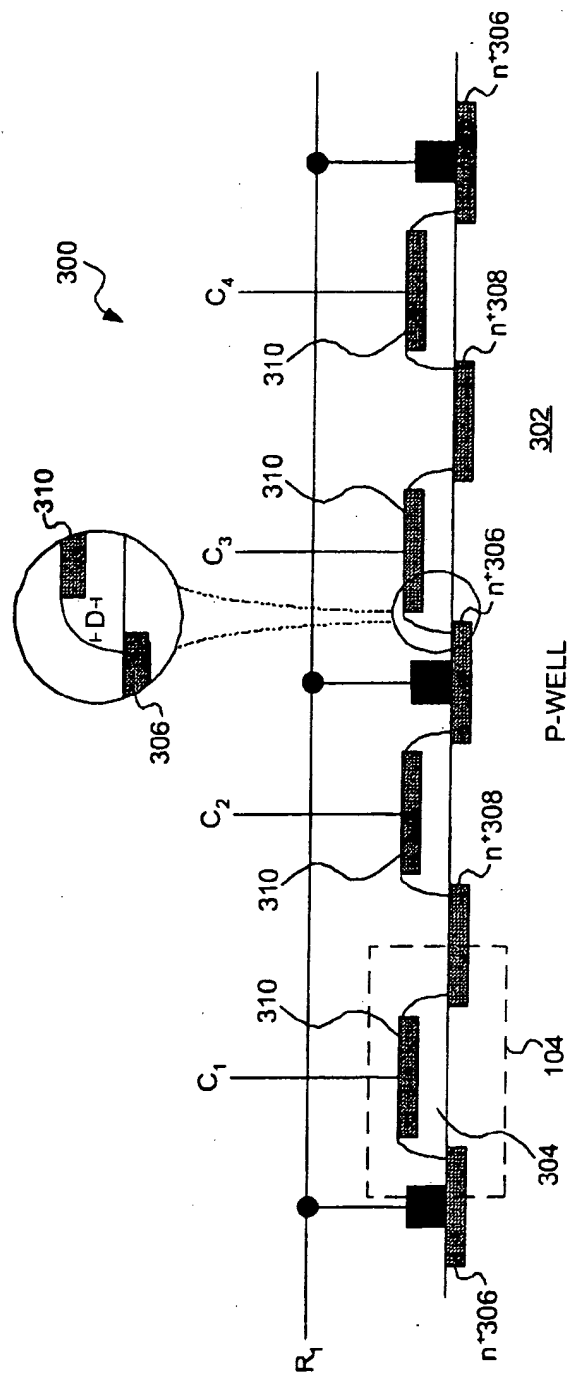


FIGURE 3

		VBL (V)	VWL (V)	PROGRAM	
PROGRAM	SC/SR	8	0	YES	401
	SC/UR	8	8	NO	403
	UC/SR	3.3	0	NO	405
	UC/UR	3.3	8	NO	407
				ISENSE	
READ	SC/SR	1.8	0	YES	409
	SC/UR	1.8	1.8	NO	411
	UC/SR	0	0	NO	413
	UC/UR	0	1.8	NO	415

FIGURE 4

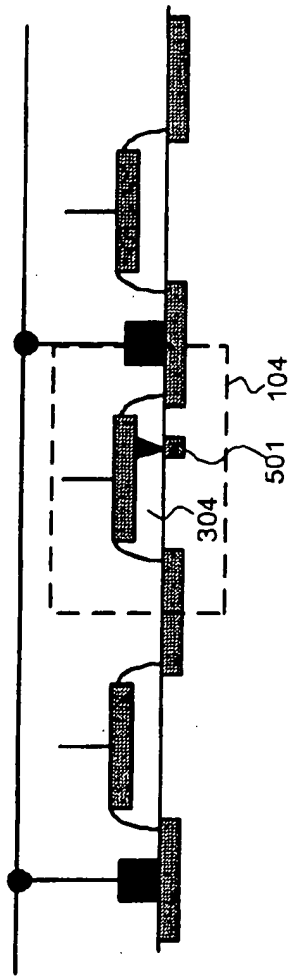


FIGURE 5

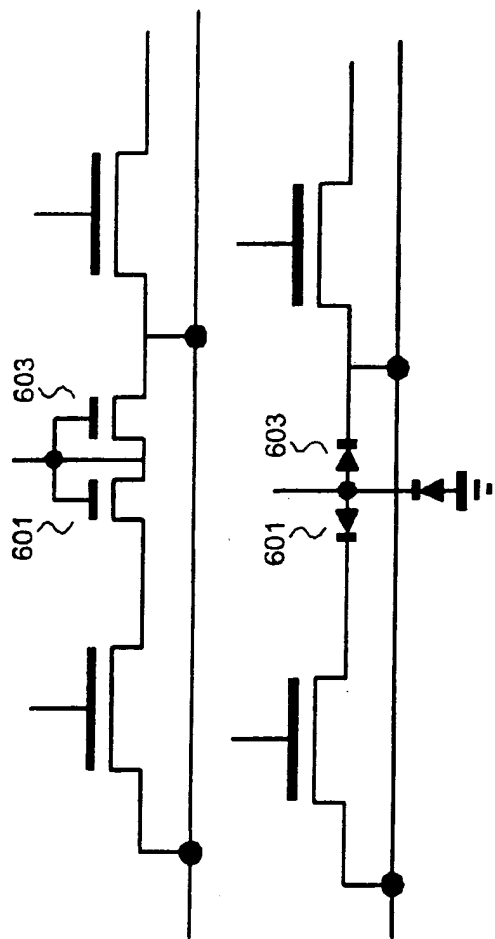


FIGURE 6

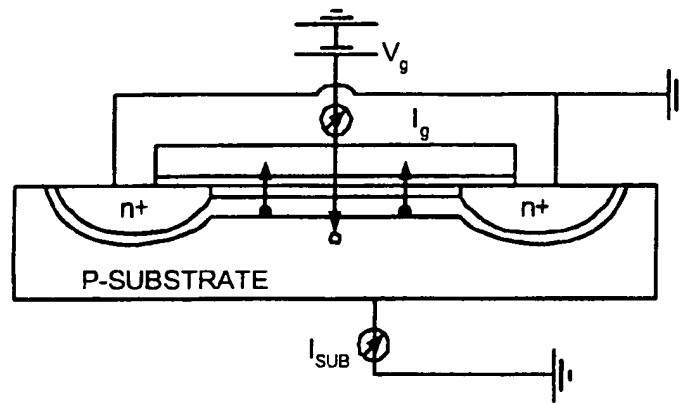


FIGURE 7

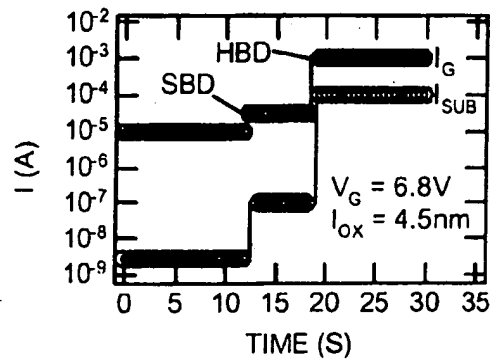


FIGURE 8

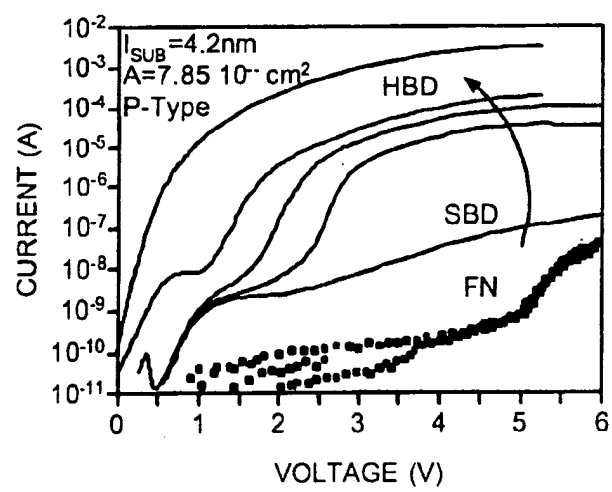


FIGURE 9

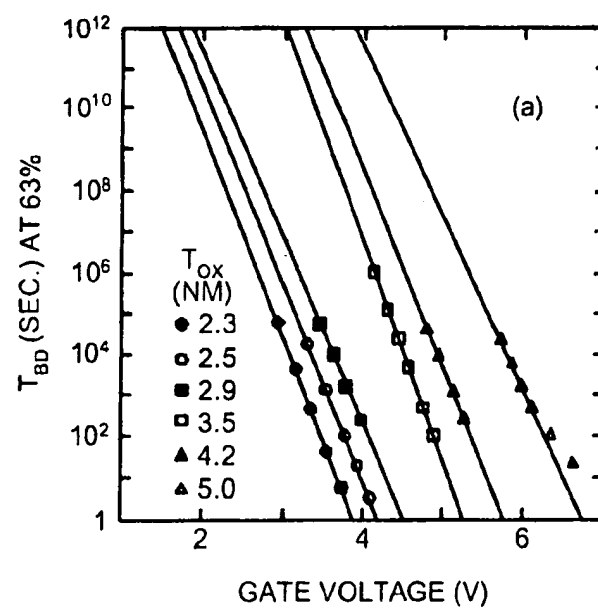


FIGURE 10

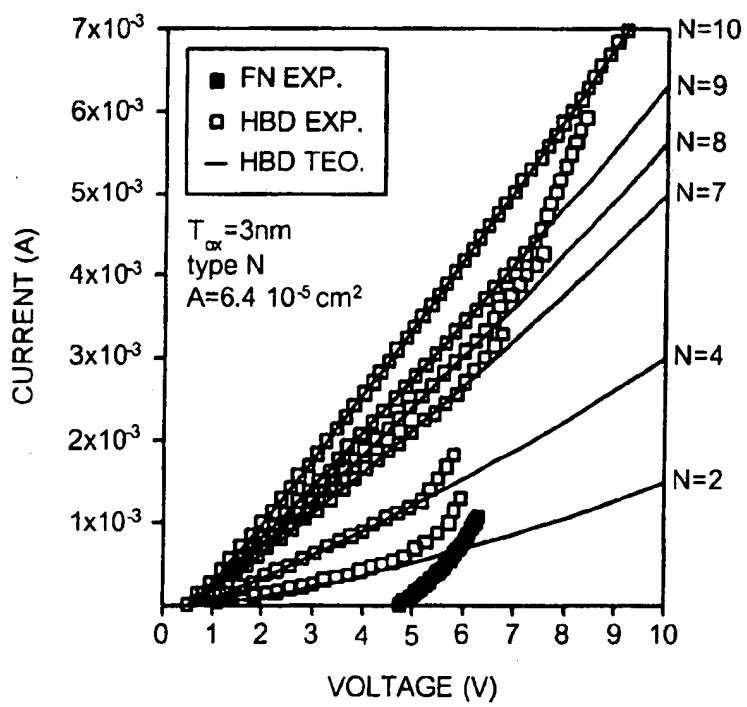


FIGURE 11

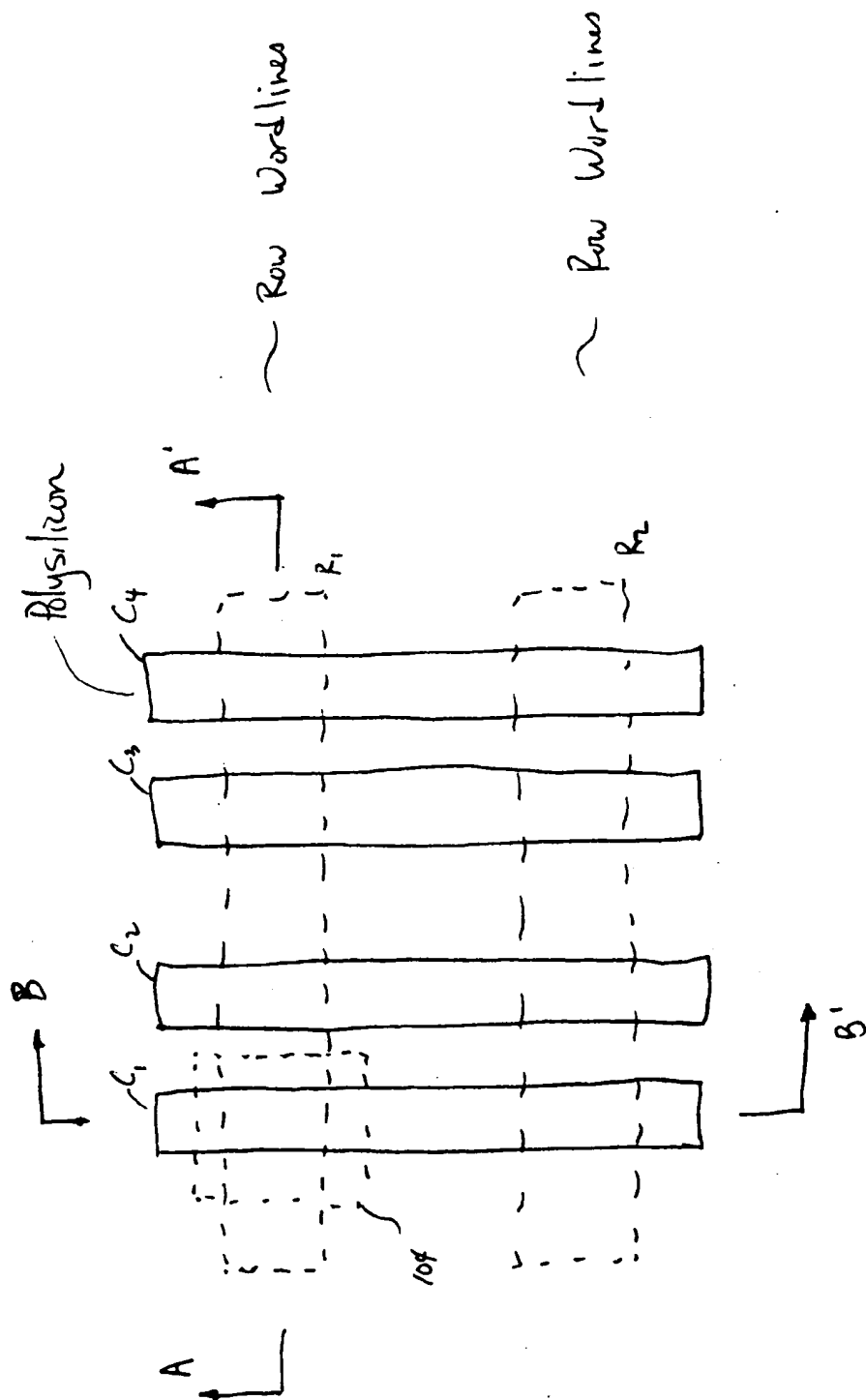


Figure 12

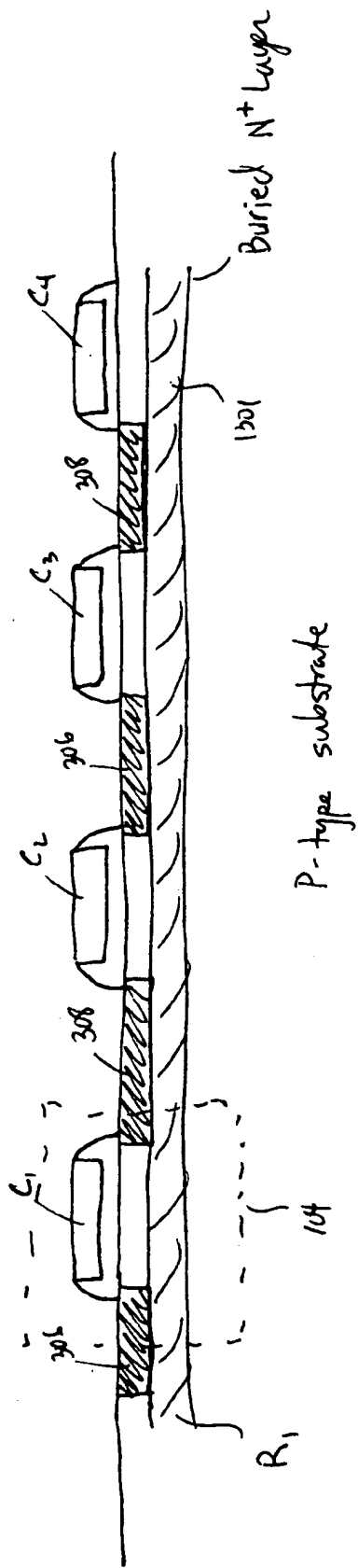


Figure 13

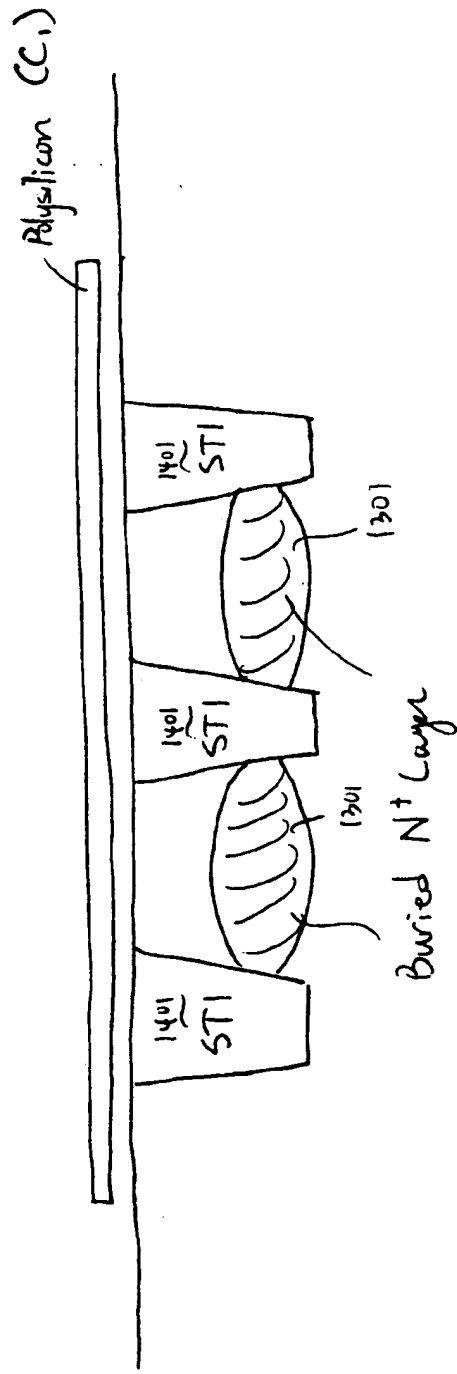


Figure 14

PROGRAM		VBL (V)	VWL (V)	PROGRAM	
	SC/SR	V_{pp}	0	YES	401
	SC/UR	V_{pp}	Floating	NO	403
	UC/SR	< 0.5	0	NO	405
	UC/UR	< 0.5	Floating	NO	407
				ISENSE	
READ	SC/SR	V_{DD} or V_{CC}	0	YES	409
	SC/UR	V_{DD} or V_{CC}	V_{DD} or V_{CC}	NO	411
	UC/SR	0 or Float	0	NO	413
	UC/UR	0 or Float	V_{DD} or V_{CC}	NO	415

FIGURE 15

Fig 16

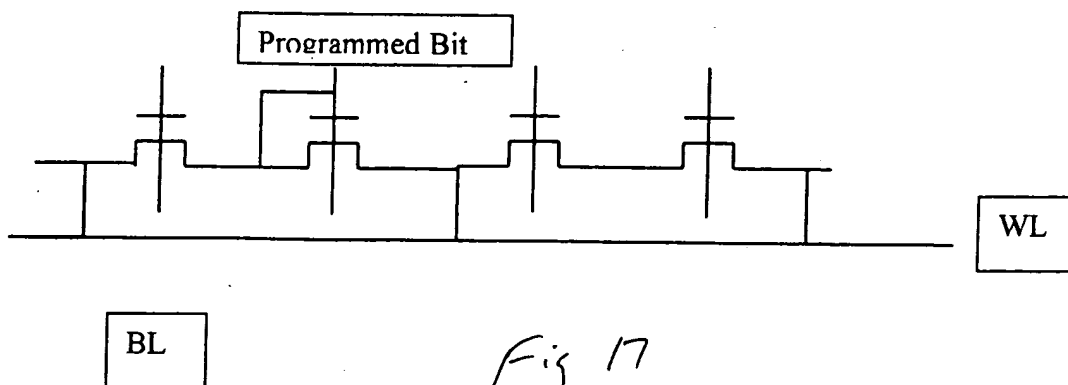
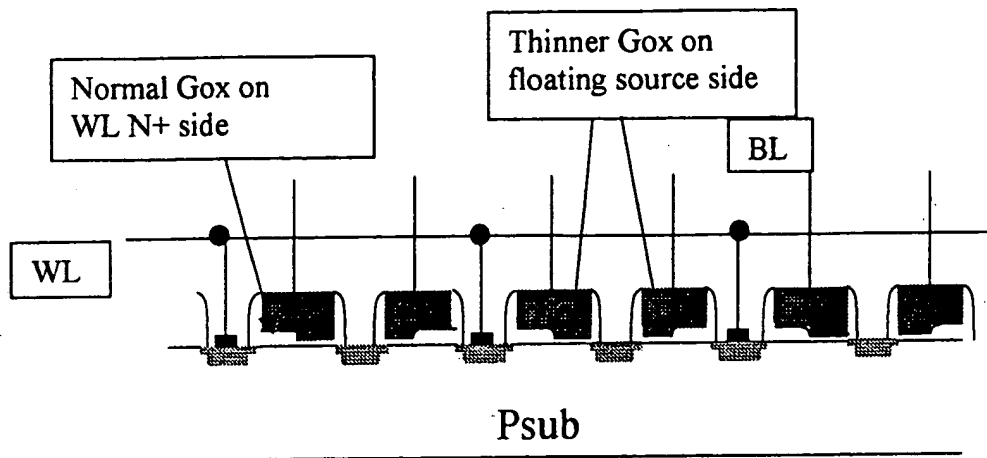


Fig 17

0.18um/0.13um XPM CX cell operation

		Vbl (V)	Vwl (V)	Program
Program	SB/SW	Vpp	0	Yes
	SB/UW	Vpp	PC to Vpp/2 and FL	No
	UB/SW	<0.5v	0	No
	UB/UW	<0.5v	PC to Vpp/2 and FL	No
				Isense
Read	SB/SW	Vdd or Vcc	0	Yes
	SB/UW	Vdd or Vcc	Vdd or Vcc	No
	UB/SW	0	0	No
	UB/UW	0	Vdd or Vcc	No

Vpp = 8~9V for Gox=32A (0.18um) or 5-7 for Gox=20A, or 3~4.5 V for 10-15A (5 to 10A thinner than normal-standard Gate oxide).

Vdd = I/O Voltage 3.3V or 2.5V

Vcc=1.8V for 0.18um and 1.2V for 0.13um

Fig 18

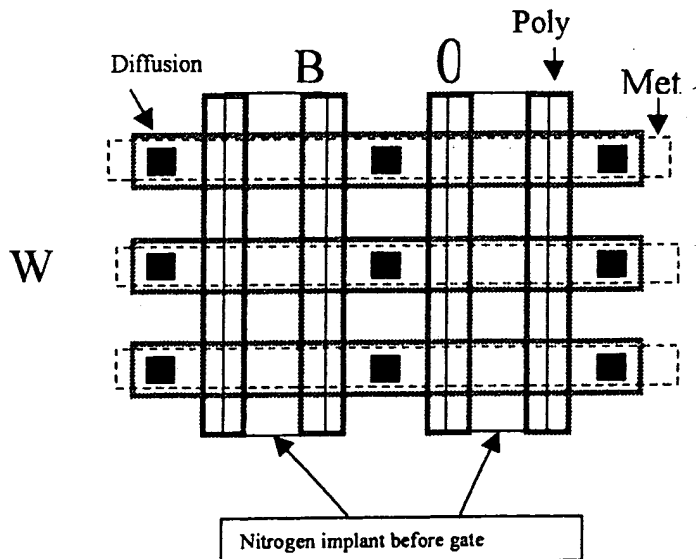


Fig 19

Step 1:

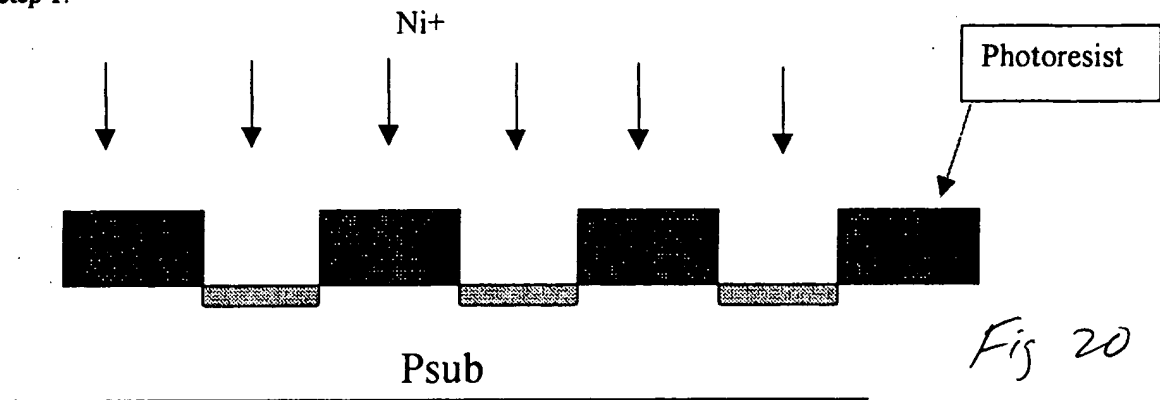


Fig 20

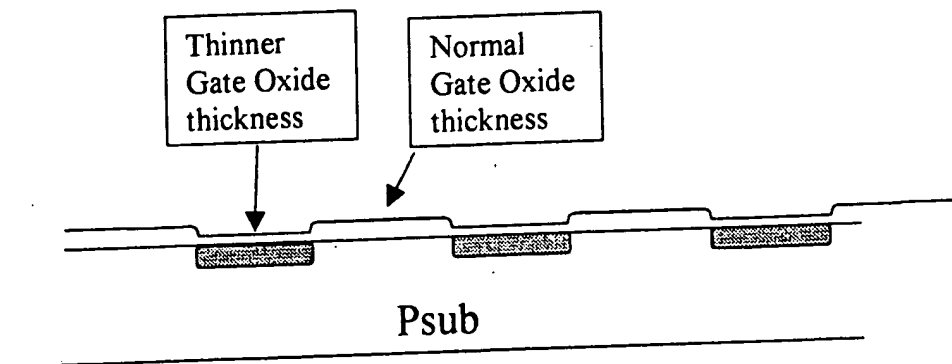


Fig 21

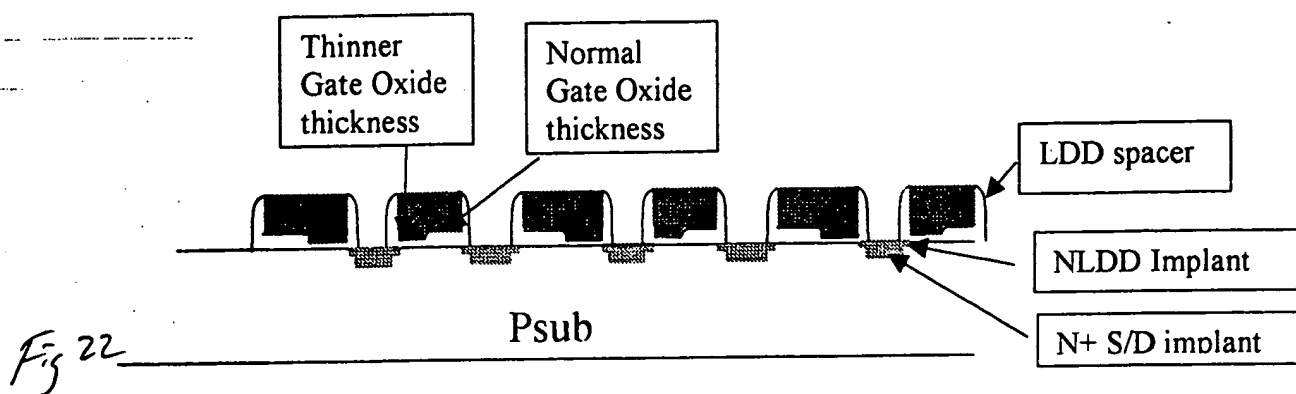


Fig 22

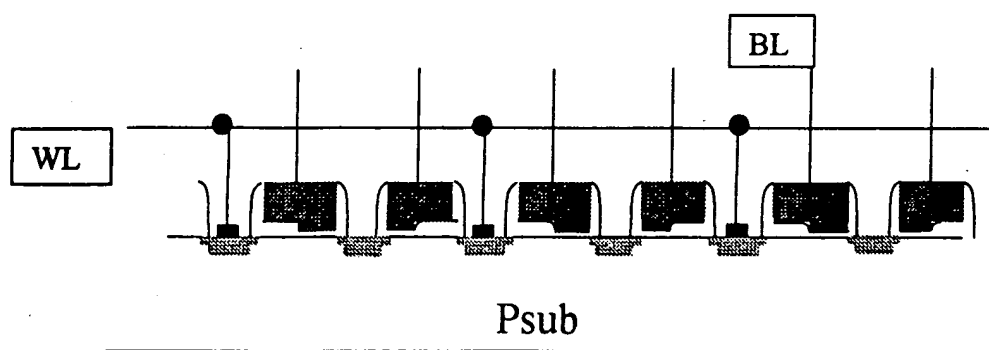


Fig 23

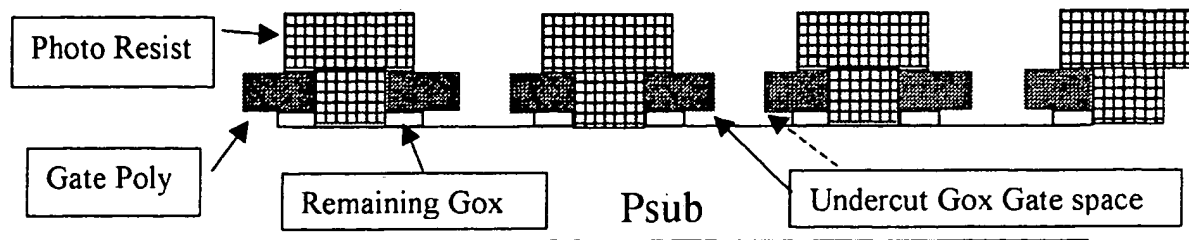


Fig. 24

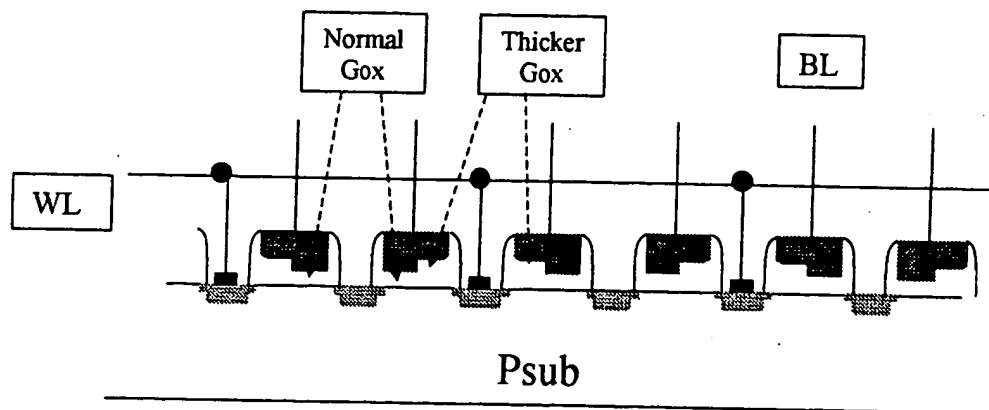


Fig 25

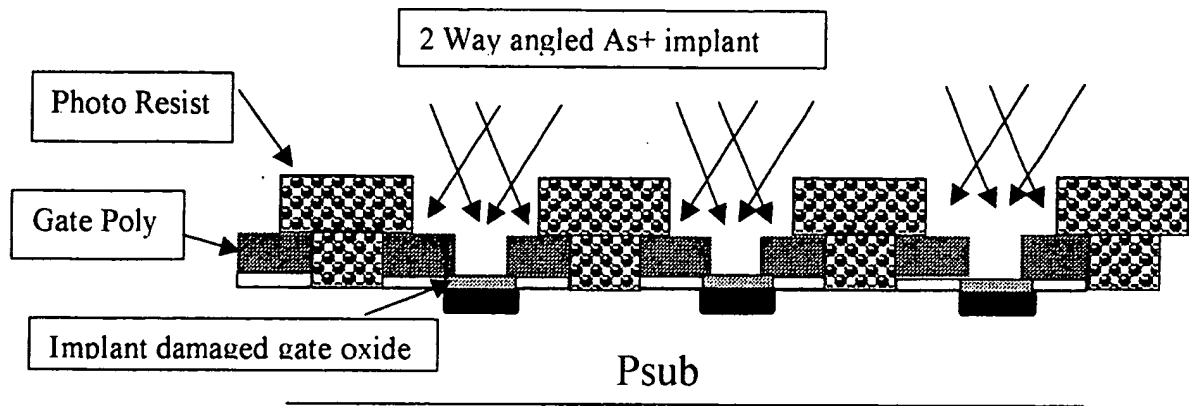


Fig 26

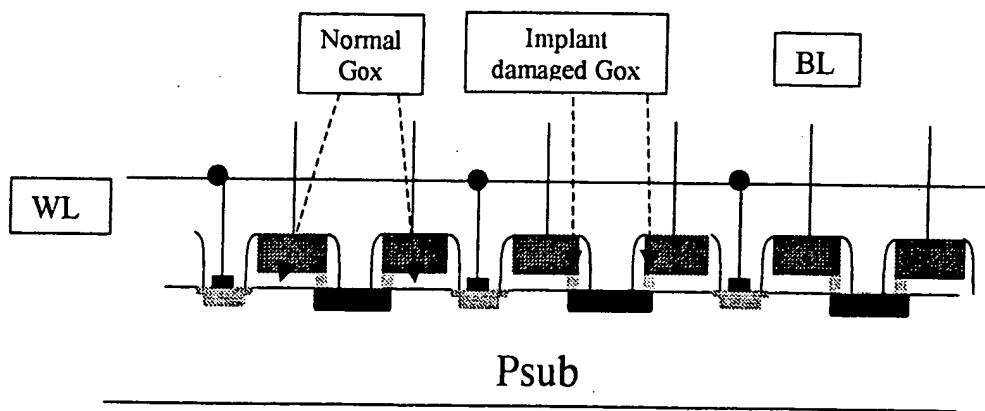


Fig 27